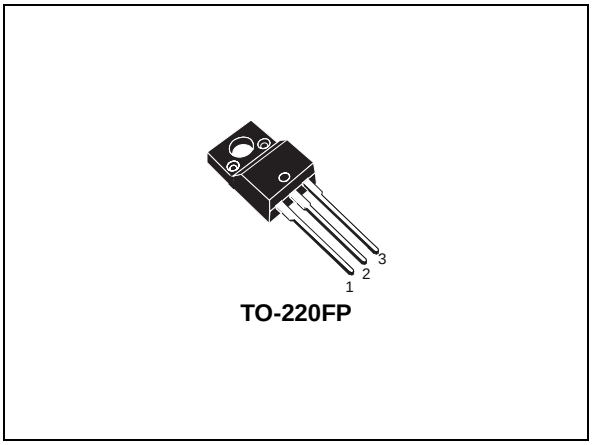
# STF34NM60N

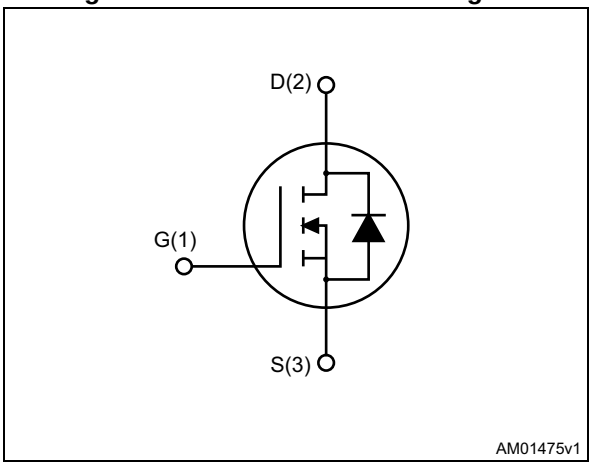
## N-channel 600 V, 0.092 Ω typ., 31.5 A MDmesh™ II Power MOSFET in a TO-220FP package

**Datasheet - production data**




**TO-220FP**

**Figure 1. Internal schematic diagram**




## Features

| Order code | $V_{DSS}$ | $R_{DS(on)}$ | $I_D$ | $P_{TOT}$ |
|---|---|---|---|---|
| STF34NM60N | 600 V | 0.105 Ω | 31.5 A | 40 W |

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

## Applications

- Switching applications

## Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

**Table 1. Device summary**

| Order code | Marking | Packages | Packaging |
|---|---|---|---|
| STF34NM60N | 34NM60N | TO-220FP | Tube |

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | 600 | V |
| $V_{GS}$ | Gate-source voltage | ± 25 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 31.5(1) | A |
| $I_D$ | Drain current (continuous) at $T_C$ = 100 °C | 20(1) | A |
| $I_{DM}$ (2) | Drain current (pulsed) | 126 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25 °C | 250 | W |
| $I_{AR}$ | Max current during repetitive or single pulse avalanche (pulse width limited by $T_{jmax}$ ) | 7 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_J$ = 25 °C, $I_D$=$I_{AS}$, $V_{DD}$= 50 V) | 345 | mJ |
| $V_{ISO}$ | Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;TC=25 °C) | 2500 | V |
| dv/dt (3) | Peak diode recovery voltage slope | 15 | V/ns |
| dv/dt(4) | MOSFET dv/dt ruggedness | 50 | V/ns |
| $T_{stg}$ | Storage temperature | -55 to 150 | °C |
| $T_j$ | Operating junction temperature | 150 | |

1. Limited by package
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 31.5$ A, di/dt $\leq$ 400 A/µs, $V_{DS}$ peak $\leq V_{(BR)DSS}$, $V_{DD}$ = 80% $V_{(BR)DSS}$
4. $V_{DS} \leq 480$ V

**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case max | 3.1 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-amb max | 62.5 | |

# 2 Electrical characteristics

($T_{CASE}$ = 25 °C unless otherwise specified).

**Table 4. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage ($V_{GS}$= 0) | $I_D$ = 1 mA | 600 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = 600 V<br>$V_{DS}$ = 600 V, Tc=125 °C | | | 1<br>100 | µA<br>µA |
| $I_{GSS}$ | Gate body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ± 25 V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2 | 3 | 4 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$= 14.5 A | | 0.092 | 0.105 | Ω |

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ =100 V, f=1 MHz, $V_{GS}$=0 | - | 2722 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 173 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 1.75 | - | pF |
| $C_{oss\ eq.}$ (1) | Equivalent capacitance time related | $V_{GS}$ = 0, $V_{DS}$ = 0 to 480 V | - | 458 | - | pF |
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 300 V, $I_D$ = 15.75 A, $R_G$=4.7 Ω, $V_{GS}$=10 V *(see Figure 18 and 14)* | - | 18 | - | ns |
| $t_r$ | Rise time | | - | 36 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 104 | - | ns |
| $t_f$ | Fall time | | - | 73 | - | ns |
| $Q_g$ | Total gate charge | $V_{DD}$ = 480 V, $I_D$ = 31.5 A $V_{GS}$ =10 V *(see Figure 15)* | - | 84 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 14 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 45 | - | nC |
| $R_G$ | Intrinsic gate resistance | f = 1 MHz, gate DC Bias=0 test signal level=20 mV open drain | - | 2.9 | - | Ω |

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$

**Table 6. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 31.5 | A |
| $I_{SDM}$(1) | Source-drain current (pulsed) | | - | | 126 | A |
| $V_{SD}$(2) | Forward on voltage | $I_{SD}$= 31.5 A, $V_{GS}$=0 | - | | 1.6 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$= 31.5 A, $V_{DD}$= 60 V di/dt = 100 A/µs, *(see Figure 16)* | - | 412 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 8 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 39 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$= 12 A,$V_{DD}$= 60 V di/dt=100 A/µs, $T_j$=150 °C *(see Figure 16)* | - | 490 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 10 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 43 | | A |

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area**

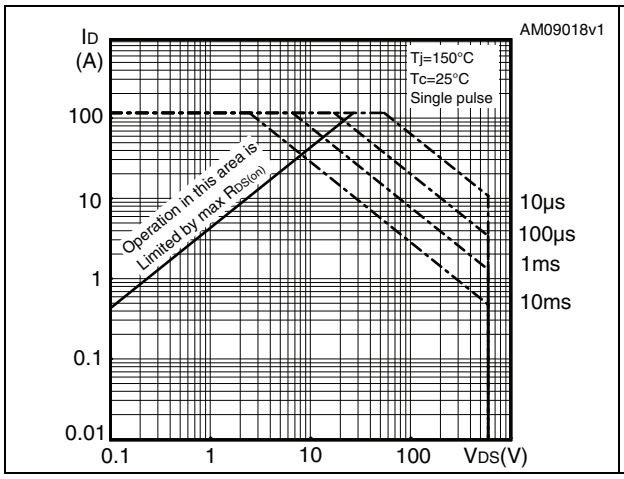



**Figure 3. Thermal impedance**

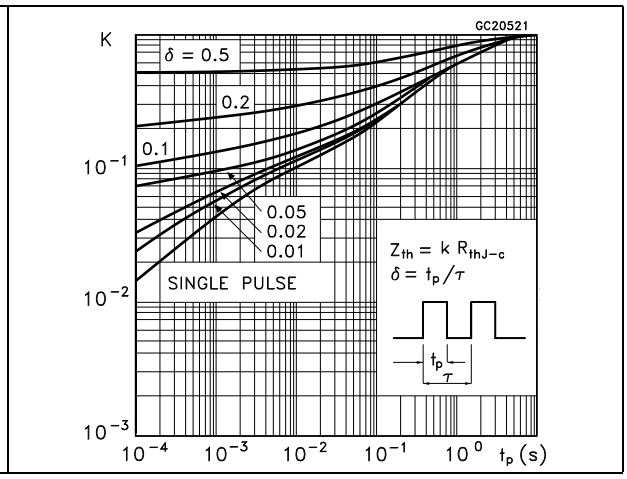



**Figure 4. Output characteristics**

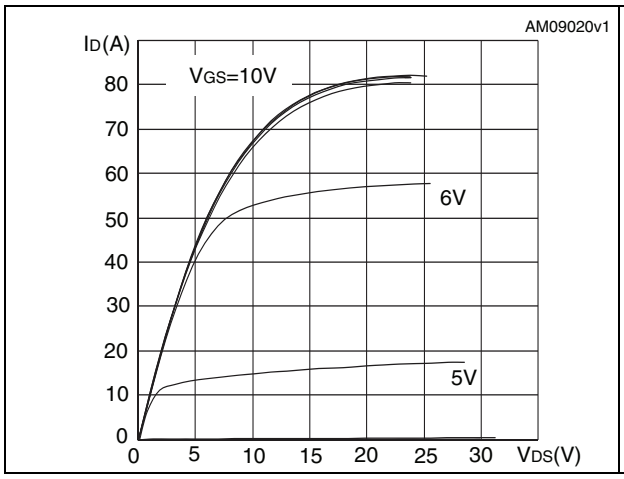



**Figure 5. Transfer characteristics**

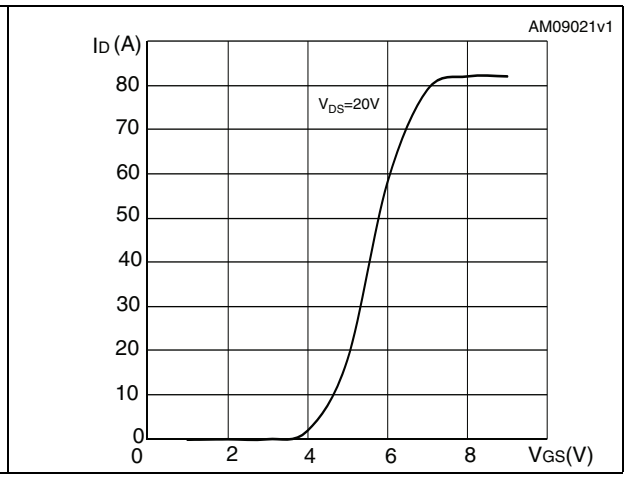



**Figure 6. Gate charge vs gate-source voltage**

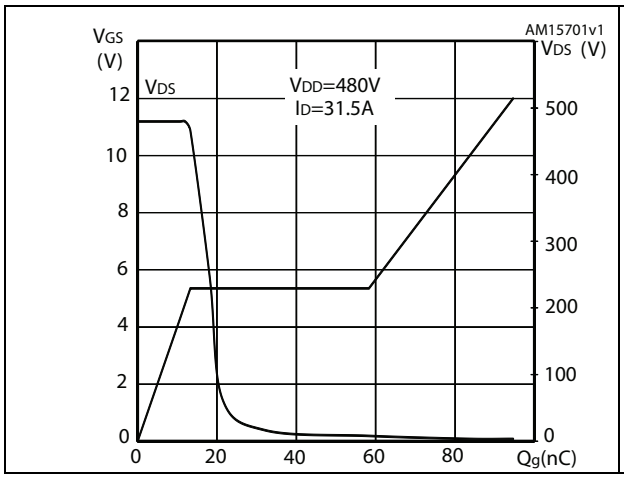



**Figure 7. Static drain-source on-resistance**

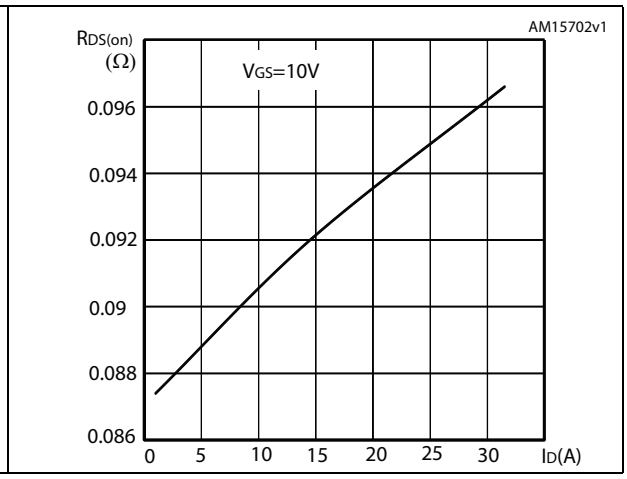


**Figure 8. Capacitance variations**

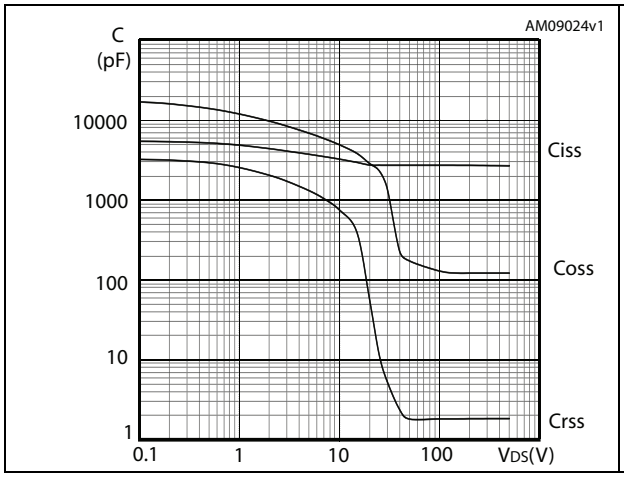



**Figure 9. Output capacitance stored energy**

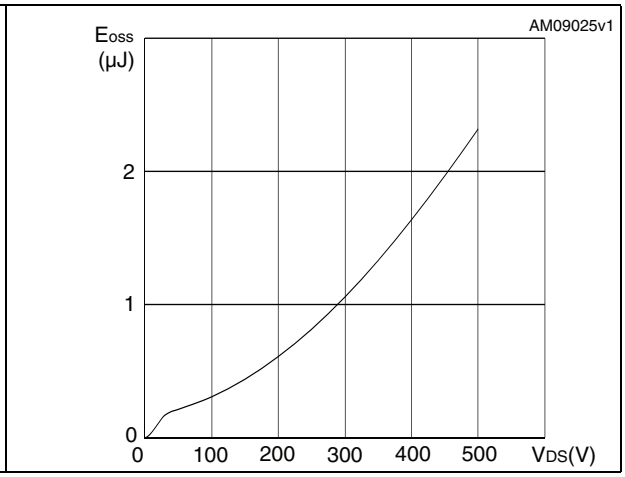



**Figure 10. Normalized gate threshold voltage vs temperature**

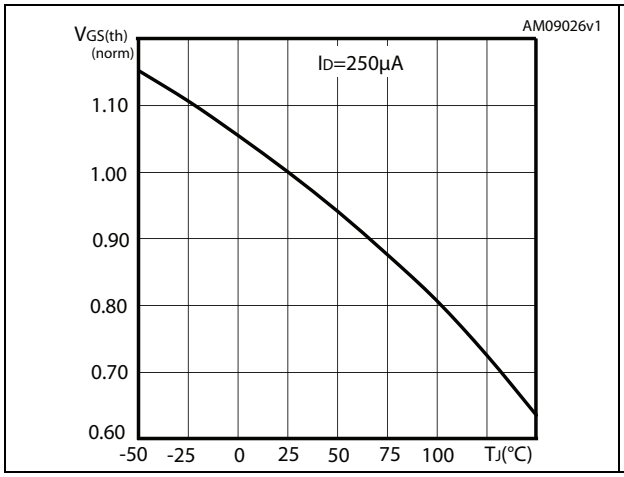



**Figure 11. Normalized on-resistance vs temperature**

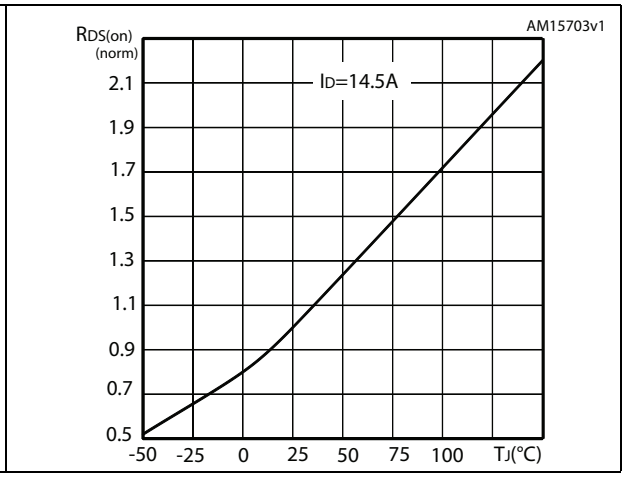



**Figure 12. Normalized $B_{VDSS}$ vs temperature**

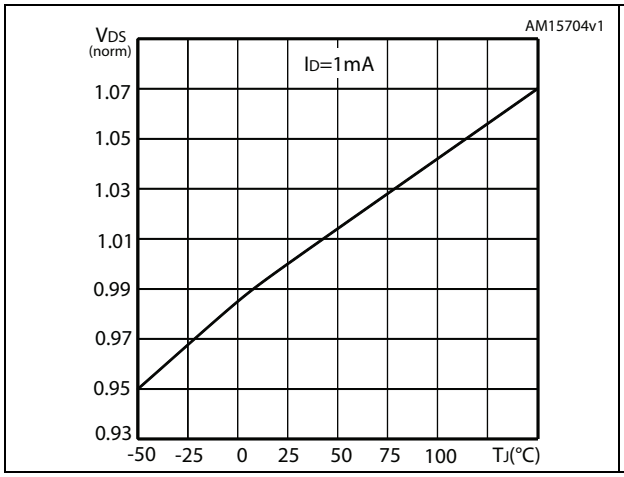
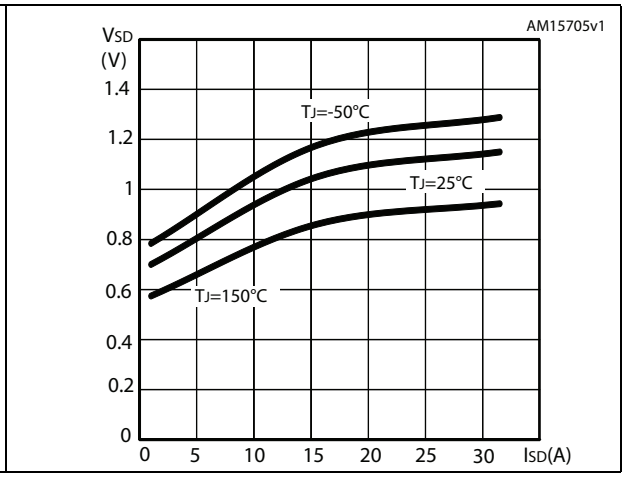



**Figure 13. Source-drain diode forward characteristics**



# 3 Test circuits

**Figure 14. Switching times test circuit for resistive load**

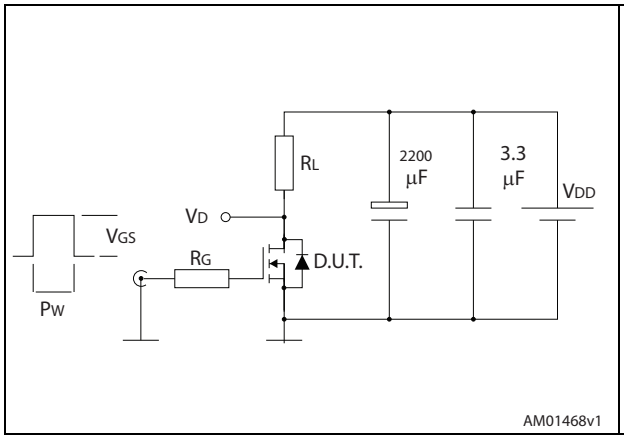



**Figure 15. Gate charge test circuit**

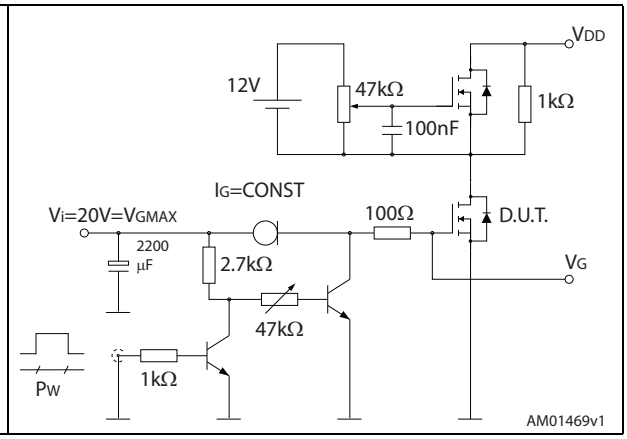



**Figure 16. Test circuit for inductive load switching and diode recovery times**

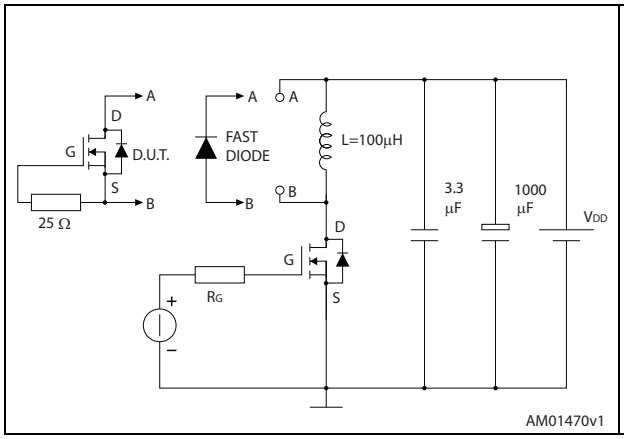



**Figure 17. Unclamped inductive load test circuit**

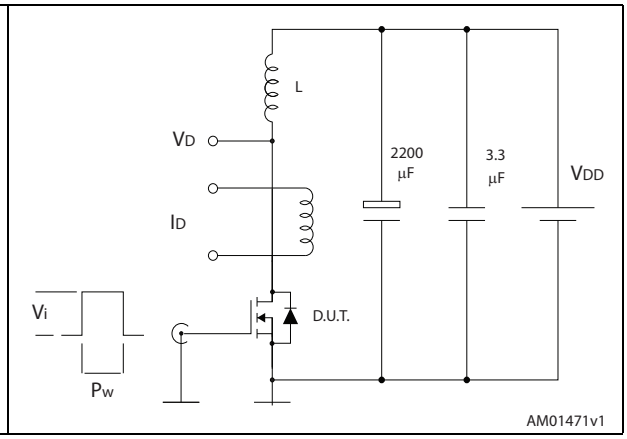



**Figure 18. Unclamped inductive waveform**

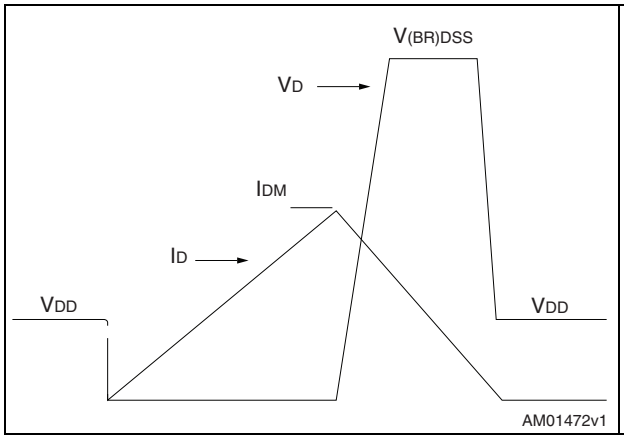
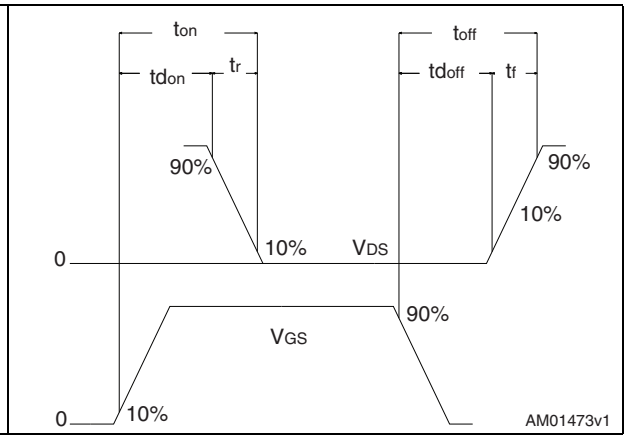



**Figure 19. Switching time waveform**



# 4 Package mechanical data

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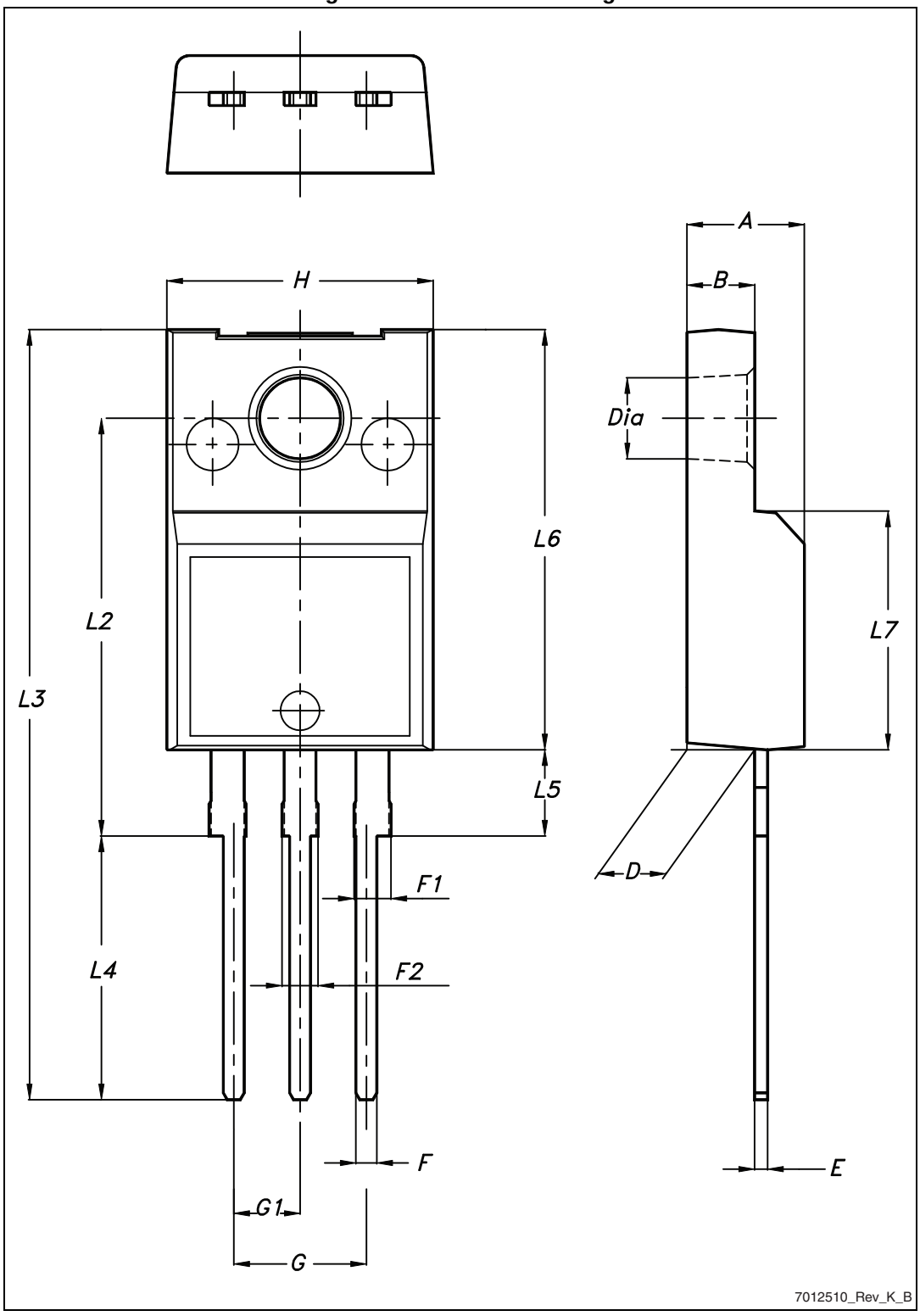
Table 7. TO-220FP mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.4 | | 4.6 |
| B | 2.5 | | 2.7 |
| D | 2.5 | | 2.75 |
| E | 0.45 | | 0.7 |
| F | 0.75 | | 1 |
| F1 | 1.15 | | 1.70 |
| F2 | 1.15 | | 1.70 |
| G | 4.95 | | 5.2 |
| G1 | 2.4 | | 2.7 |
| H | 10 | | 10.4 |
| L2 | | 16 | |
| L3 | 28.6 | | 30.6 |
| L4 | 9.8 | | 10.6 |
| L5 | 2.9 | | 3.6 |
| L6 | 15.9 | | 16.4 |
| L7 | 9 | | 9.3 |
| Dia | 3 | | 3.2 |

Figure 20. TO-220FP drawing



# 5 Revision history

Table 8. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 16-Jul-2013 | 1 | First release. |

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