

MOSFETs Silicon N-Channel MOS

SSM3K72CFS

1. Applications

· High-Speed Switching

2. Features

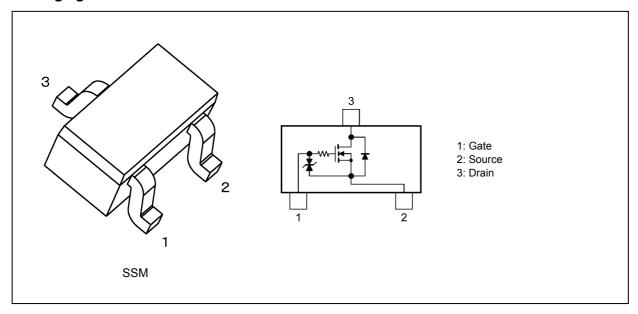
- (1) ESD protected gate
- (2) Low drain-source on-resistance

 $: R_{DS(ON)} = 2.8 \Omega \text{ (typ.) } (@V_{GS} = 10 \text{ V})$

 $R_{\mathrm{DS(ON)}} = 3.1~\Omega~\mathrm{(typ.)}~(@V_{\mathrm{GS}} = 5.0~\mathrm{V})$

 $R_{\mathrm{DS(ON)}} = 3.2~\Omega~\mathrm{(typ.)}~(@V_{\mathrm{GS}} = 4.5~\mathrm{V})$

3. Packaging and Internal Circuit





4. Absolute Maximum Ratings (Note) (Unless otherwise specified, Ta = 25 °C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	60	V
Gate-source voltage		V_{GSS}	±20	
Drain current (DC)	(Note 1)	I_D	170	mA
Drain current (pulsed)	(Note 1), (Note 2)	I _{DP}	680	
Power dissipation	(Note 3)	P_{D}	150	mW
Power dissipation	(Note 4)		500	
Channel temperature		T _{ch}	150	ů
Storage temperature		T _{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

- Note 1: Ensure that the channel temperature does not exceed 150 °C.
- Note 2: Pulse width \leq 10 μ s, Duty \leq 1 %
- Note 3: Device mounted on a 25.4 mm \times 25.4 mm \times 1.6 mm FR4 glass epoxy board (Cu pad: 0.36 mm² \times 3)
- Note 4: Device mounted on a 25.4 mm × 25.4 mm × 1.6 mm FR4 glass epoxy board (Cu pad: 645 mm²)
- Note: This transistor is sensitive to electrostatic discharge and should be handled with care.
- Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.
- Note: The channel-to-ambient thermal resistance, R_{th(ch-a)}, and the drain power dissipation, P_D, vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.



5. Electrical Characteristics

5.1. Static Characteristics (Unless otherwise specified, T_a = 25 °C)

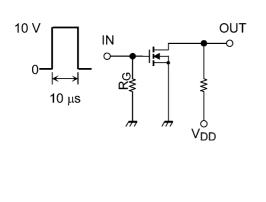
Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 16 \text{ V}$	_	_	±2	μА
		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 10 \text{ V}$	_	_	±0.5	
		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 5 \text{ V}$	_	_	±0.1	
Drain cut-off current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V	_	_	1	
		$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V},$ $T_j = 150 \text{ °C}$	_	_	200	
Drain-source breakdown voltage	V _{(BR)DSS}	$I_D = 250 \mu A, V_{GS} = 0 V$	60	_	_	V
Gate threshold voltage	V _{th}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.1	_	2.1	
Drain-source on-resistance (Note 1) R _{DS(ON)}	I _D = 100 mA, V _{GS} = 4.5 V	_	3.2	4.7	Ω
		I _D = 100 mA, V _{GS} = 5.0 V	_	3.1	4.4	
		I _D = 100 mA, V _{GS} = 10 V	_	2.8	3.9	
		I_D = 100 mA, V_{GS} = 10 V, T_j = 150 °C	_	5.4	8.1	
Forward transfer admittance (Note 1) Y _{fs}	V _{DS} = 10 V, I _D = 200 mA	_	450	_	mS

Note 1: Pulse measurement.

5.2. Dynamic Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input capacitance	C _{iss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V},$	_	11	17	pF
Reverse transfer capacitance	C _{rss}	f = 1 MHz	_	0.7	_	
Output capacitance	C _{oss}		_	3	_	
Switching time (rise time)	t _r	V _{DD} = 40 V, I _D = 160 mA,		3	_	ns
Switching time (turn-on delay time)	t _{d(on)}	V_{GS} = 0 to 10 V, R _G = 50 Ω Duty ≤ 1%, V _{IN} : t _r , t _f < 5 ns,	_	2	4	
Switching time (fall time)	t _f	Common source,		24	_	
Switching time (turn-off delay time)	t _{d(off)}	See Chapter 5.3.		7	14	

5.3. Switching Time Test Circuit





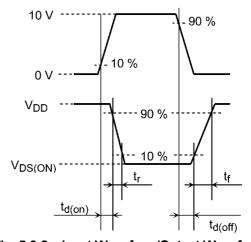


Fig. 5.3.2 Input Waveform/Output Waveform



5.4. Gate Charge Characteristics (Unless otherwise specified, T_a = 25 °C)

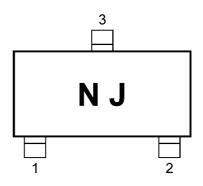
Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Total gate charge (gate-source plus gate-drain)		V_{DD} = 30 V, I_{D} = 200 mA,	_	0.27	0.35	nC
Gate-source charge	Q _{gs}	V _{GS} = 4.5 V	_	80.0	_	
Gate-drain charge	Q _{gd}		_	0.08	_	

5.5. Source-Drain Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Diode forward voltage (No	ote 1)	V_{DSF}	$I_D = -115 \text{ mA}, V_{GS} = 0 \text{ V}$		-0.87	-1.2	V

Note 1: Pulse measurement.

6. Marking



7. Characteristics Curves (Note)

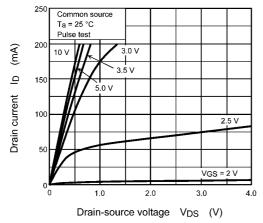
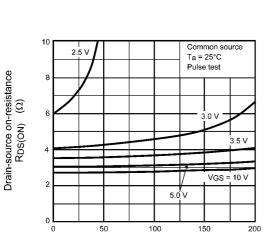


Fig. 7.1 $I_D - V_{DS}$



Drain current ID (mA)

Fig. 7.3 RDS(ON) - ID

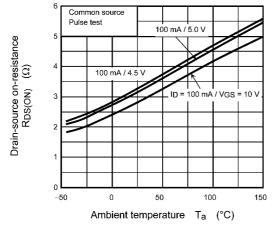


Fig. 7.5 R_{DS(ON)} - T_a

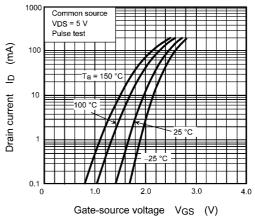


Fig. 7.2 I_D - V_{GS}

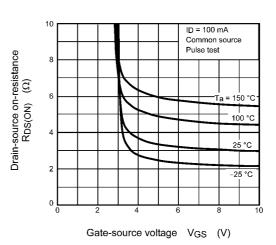


Fig. 7.4 R_{DS(ON)} - V_{GS}

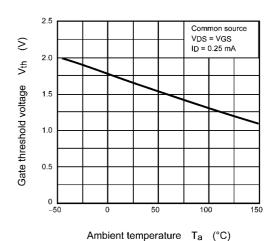


Fig. 7.6 V_{th} - T_a

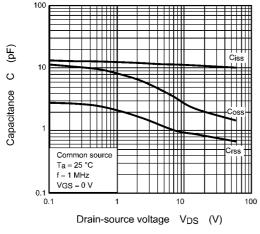


Fig. 7.7 C - V_{DS}

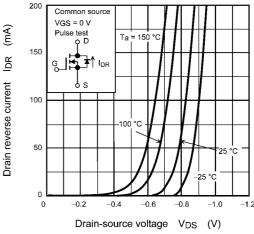


Fig. 7.8 I_{DR} - V_{DS}

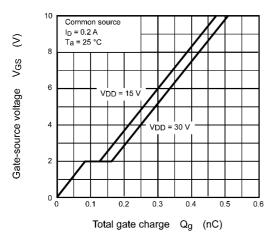


Fig. 7.9 Dynamic Input Characteristics

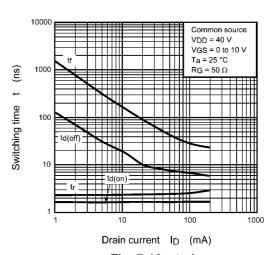


Fig. 7.10 t-I_D

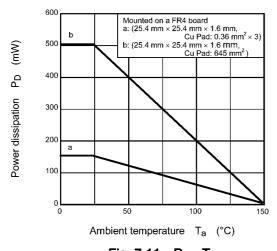


Fig. 7.11 P_D - T_a

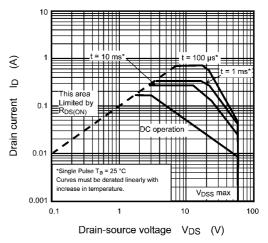


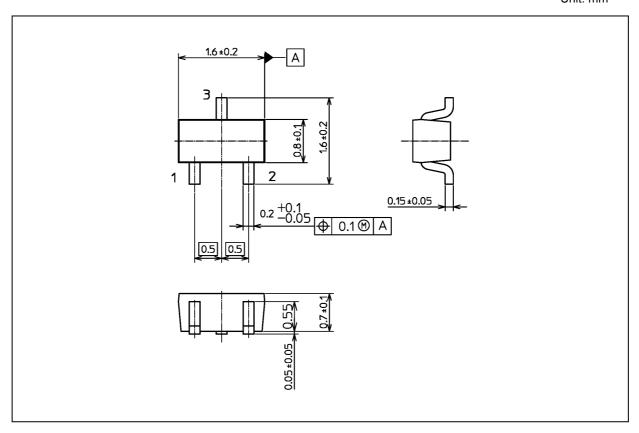
Fig. 7.12 Safe Operating Area

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



Package Dimensions

Unit: mm



Weight: 2.4 mg (typ.)

	Package Name(s)
JEDEC: SOT-416	
Nickname: SSM	



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